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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/699,537	10/30/2000	Walter L. Moden	2687.3US (94-305.3)	8772

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EXAMINER	
BROCK II, PAUL E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 12/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/699,537	MODEN, WALTER L.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5,8,12,26,30,33 and 37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5,8,12,26,30,33 and 37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *22*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the two semiconductor chips mounted to a first substrate further being mounted to a second substrate, and a semiconductor chip mounted to a substrate having a plurality of vias there through must be shown or the feature(s) canceled from the claim(s). Further, "connecting said second substrate to said first substrate having said send located soley on one side of the first substrate without any portion of the first substrate being located below said upper surface of the second substrate and portions of said plurality of bond wires extending between the die side surface of said second substrate and a die side surface of said first substrate, the connections between said first substrate and said second substrate formed by one of a plurality of solder balls and a plurality of pins" must be shown or the feature(s) canceled from the claim(s).No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 1, 5, 8, 12, 26, 30, 33, and 37 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

With specific regard to claim 1, it is not clear where in the originally filed specification there is support for: "connecting said second substrate to said first substrate having said send located soley on one side of the first substrate without any portion of the first substrate being located below said upper surface of the second substrate and portions of said plurality of bond wires extending between the die side surface of said second substrate and a die side surface of said first substrate, the connections between said first substrate and said second substrate formed by one of a plurality of solder balls and a plurality of pins." Applicant states these features can be found on page 5, lines 8 – 12 of the originally filed specification. The combination of these specific features are not disclosed, described or suggested in this cited passage or anywhere else in the originally filed disclosure. Further, it is not clear where in the originally filed specification support for "second substrate having an upper surface without recesses therein" can be found.

With specific regard to claim 5, it is not clear where in the originally filed specification there is support for "said upper surface [of said master board] having no recesses therein." [emphasis added].

With specific regard to claim 8, it is not clear where in the originally filed specification there is support for "said upper surface [of said second substrate] having no recesses therein for a semiconductor die." [emphasis added].

With specific regard to claim 12, it is not clear where in the originally filed specification there is support for ""the upper surface [of the master board] being free of semiconductor die recesses therein." [emphasis added].

With specific regard to claim 26, it is not clear where in the originally filed specification there is support for "a second substrate having an upper surface free of recesses for semiconductor die."

With specific regard to claim 30, it is not clear where in the originally filed specification there is support for "said upper surface [of said master board] free of any recess for the receipt of a semiconductor die therein." [emphasis added].

With specific regard to claim 33, it is not clear where in the originally filed specification there is support for "said upper surface [of said second substrate] without any recess for the receipt of at least one semiconductor die." [emphasis added].

With specific regard to claim 37, it is not clear where in the originally filed specification there is support for "said upper surface [of said master board] being free of semiconductor die recesses therein." [emphasis added].

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "said plurality of bond wires extending between the die side surface of said second substrate and a die side surface of said first substrate" in lines 22 – 24. There is insufficient antecedent basis for this limitation in the claim. For purposes of this office action "said plurality of bond wires extending between the die side surface of said second substrate and a die side surface of said first substrate" will be considered --a plurality of bond wires extending between the die side surface of said second substrate and a die side surface of said first substrate--.

With regard to claim 26, it is not clear if "said substrate" in line 18 is the first or second substrate. For purposes of this office action "said substrate" will be considered --said first substrate--.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eide (USPAT 5313096) in view of Kohno et al. (USPAT 5293068, Kohno) and Lin et al. (USPAT 5239198, Lin).

With regard to claim 1, Eide discloses in figure 10 providing a semiconductor die (20) having a surface having a plurality of bond pads (36) extending along an axis of the die on the surface. Eide discloses in figure 10 providing a second substrate (24) having a die side surface, a

second attachment surface, at least one via (40 or 38) extending through the substrate from the die side surface to the second attachment surface, a plurality of circuits (46), and a plurality of bond pads (56) located on the second attachment surface of the second substrate. Eide discloses in figures 10, 11 and column 7, lines 19 – 22 applying an adhesive to a portion of the die sides of the first substrate to attach the semiconductor die thereto. Eide discloses in figure 10 attaching the surface having a plurality of bond pads thereon of the semiconductor die to the die side surface of the second substrate so that the semiconductor die is located above the substrate (turn sheet 4 of 6 of Eide upside-down). Eide discloses in figure 10 connecting the plurality of bond pads of the semiconductor die to the plurality of bond pads on the second attachment surface of the substrate using a plurality of wire bonds (72), the plurality of wire bonds extending through the at least one via extending through the second substrate. Eide discloses in figures 7 and 11 filling at least a portion of the via in the substrate with a sealant. Eide does not teach that the plurality of bond pads extend along a longitudinal axis. Kohno teaches in figures 3 and 4 a plurality of bond pads (1p) extending along a longitudinal axis of a die (1) on a surface of the die. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the longitudinal layout of bond pads of Kohno in the method of Eide in order to simplify a layout of bond pads. Eide and Kohno do not teach connection the second substrate to a first substrate, or a plurality of bond pads located on the second attachment surface and on the die side of the second substrate. As best the examiner can ascertain, Lin teaches in figure 4 connecting a second substrate (12), having a plurality of bond pads located on a second attachment surface and on a die side of the second substrate, to a first substrate (38) having the second located soley on one side of the first substrate without any portion of the first substrate

being located below the upper surface of the second substrate and portions of a plurality of bond wires (22) extending between a die side surface of the second substrate and a die side surface of the first substrate, the connections between the first substrate and the second substrate formed by one of a plurality of solder balls (32). It would have been obvious to use the plurality of bonds pads of the second substrate, the entire first substrate, and connecting of Lin in the method of Eide and Kohne in order to provide external electrical connections to the device as stated by Lin in column 2, lines 44 – 50.

Claim 26 is rejected similar to claim 1 wherein the first substrate and the second substrate of claim 1 correspond to the second substrate and the first substrate of claim 26, respectively.

8. Claims 5 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eide in view of Lin.

Eide discloses in figures 10 and 11 a method of electrically connecting a semiconductor die (20) to a substrate (24).

With regard to claim 5, Eide discloses in figures 8, 10 and 11 providing a semiconductor die having a plurality of bond pads (36) thereon. Eide discloses in figures 8, 10 and 11 providing a board (24) having a die side surface, a second attachment surface, a plurality of vias (38 and 40) extending through the board from the die side surface to the second attachment surface, a plurality of circuits (46), and a plurality of bond pads (56) located on the second attachment surface of the board. Eide discloses in figures 8, 10 and 11 attaching the semiconductor die (20) to a portion of the die side surface of the board. Eide discloses in figures 8, 10 and 11 connecting the plurality of bond pads of the semiconductor die to the plurality of

connection points of the board using a plurality of wire bonds (72), the plurality of wire bonds extending through the plurality of vias extending through the board. Eide does not disclose connecting the board to a master board using a plurality of electrical connectors on the board. Lin teaches in figure 4 providing a master board (38) having a plurality of circuit traces (40) on an upper surface thereof, the upper surface having no recesses therein. Lin teaches in figure 4 providing a plurality of electrical connectors (16) for connecting a plurality of connection points located on a second attachment surface of a board (12) to the circuit traces of the master board. Lin teaches in figure 4 connecting the board and master board using the plurality of electrical connectors on the board to the plurality of circuit traces on the master board using a plurality of solder balls, the board being located above the upper surface of the master board. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the master board, connection points, and solder balls of Lin in the method of Eide in order to provide external electrical connections to the device as stated by Lin in column 2, lines 44 – 50.

Claim 30 is rejected similar to claim 5.

9. Claims 8, 12, 33 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kryzaniwsky (USPAT 5099309) in view of Kohno and Lin.

With regard to claim 8, Kryzaniwsky discloses in figures 1a – 11 a method of electrically connecting at least two semiconductor die (5 and 7) to a substrate (40). Kryzaniwsky discloses in figures 1a – 11 providing at least two semiconductor die, each semiconductor die having a surface having a plurality of bond pads extending along an axis of the die on the surface. Kryzaniwsky discloses in figure 9 providing a substrate having a die side surface, a second

attachment surface, at least two vias extending through the substrate from the die side surface to the second attachment surface, a plurality of circuits (12), and a plurality of connection points located on the second attachment surface of the board. Kryzaniwsky discloses in figures 1a – 1l and column 3, lines 35 – 37 applying an adhesive to a portion of the die side of the substrate to attach each semiconductor die thereto. Kryzaniwsky discloses in figures 1a – 1l attaching the surface having a plurality of bond pads thereon of a semiconductor die of the at least two semiconductor die to the die side surface of the substrate having the plurality of bond pads of the semiconductor die located over one of the at least two vias extending through the substrate. Kryzaniwsky discloses in figures 1a – 1l filling at least a portion of each via in the substrate with a sealant (42). Kryzaniwsky discloses in figures 1a – 1l connecting (20 and 21) the plurality of bond pads of the semiconductor die to the plurality of connection points of the substrate using a plurality of wire bonds, the plurality of wire bonds extending through the one via extending through the substrate of the at least two vias extending through the substrate. Kryzaniwsky does not disclose that the connection points are bond pads. Kohno discloses in figure 4 bond pads on a second attachment surface of a substrate (2). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the bond pads of Kohno as the connection points of Kryzaniwsky in order to have a dedicated surface in which to bond a wire to as is well known in the art. Kohno further teaches the plurality of bond pads extend along a longitudinal axis of the die of the surface of the semiconductor die. It would have further been obvious to one of ordinary skill in the art to arrange the bond pads of Kryzaniwsky in the longitudinal direction of Kohno in order to simplify the layout of the bond pads. It is not clear if Kryzaniwsky and Kohno teach a second substrate. Lin teaches in figure 4 connecting at least two

semiconductor die (20 and 27) to a first substrate (12) for connection to circuit traces (40) on the upper surface of a second substrate (38), the upper surface having no recesses therein for a semiconductor die. Lin teaches in figure 4 a second attachment surface having bond pads (16) for the at least two semiconductor die electrical connection with traces on an upper surface of a second substrate using a plurality of solder balls (32), the first substrate for locating above the upper surface of the second substrate. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the second substrate and bond pads of Lin in the method of Kryzaniwsky and Kohno in order to provide external electrical connections to the device as stated by Lin in column 2, lines 44 – 50.

Claim 33 is rejected similar to claim 8.

With regard to claim 12, Kryzaniwsky discloses in figures 1a – 1l a method of electrically connecting a plurality of semiconductor die (5 and 7) to a master board (40). Kryzaniwsky discloses in figures 1a – 1l providing a plurality of semiconductor die, each semiconductor die being a semiconductor die having a plurality of bond pads extending along an axis of the die on the surface and a semiconductor die having a surface having a plurality of bond pads extending in a leads-over configuration on the surface. Kryzaniwsky discloses in figure 9 providing a board having a die side surface, a second attachment surface, a plurality of vias extending through the board from the die side surface to the second attachment surface, a plurality of circuits (12), and a plurality of connection points located on the second attachment surface of the board. Kryzaniwsky discloses in figures 1a – 1l attaching each semiconductor die of the plurality of semiconductor die to a portion of the dies side surface of the board. Kryzaniwsky discloses in figures 1a – 1l connecting (20 and 21) the plurality of bond pads of the semiconductor die to the

plurality of connection points of the board using a plurality of wire bonds, the plurality of wire bonds extending through plurality of vias extending through the board. Kryzaniwsky does not disclose that the connection points are bond pads. Kohno discloses in figure 4 bond pads on a second attachment surface of a substrate (2). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the bond pads of Kohno as the connection points of Kryzaniwsky in order to have a dedicated surface in which to bond a wire to as is well known in the art. Kohno further teaches the plurality of bond pads extend along a longitudinal axis of the die of the surface of the semiconductor die. It would have further been obvious to one of ordinary skill in the art to arrange the bond pads of Kryzaniwsky in the longitudinal direction of Kohno in order to simplify the layout of the bond pads. It is not clear if Kryzaniwsky and Kohno discloses a master board or providing. Lin in figure 4 providing a master board having a plurality of circuit traces located on an upper surface thereof, the upper surface being free of any recess for the location of a semiconductor device therein; providing a plurality of electrical connectors for connecting a plurality of bond pads located on a second attachment surface of a board to circuit traces of the master board; and connecting the board and master board using the plurality of electrical connectors on the board to the plurality of circuit traces on the master board using a plurality of solder balls, the board being located above the upper surface of the master board. It would have been obvious to one of ordinary skill in the art that electrical connectors and master board of Lin in the method of Kryzaniwsky and Kohno in order to create an external connection means between a plurality of semiconductor devices and packages.

Claim 37 is rejected similarly to claim 12.

Response to Arguments

10. Applicant's arguments filed April 15, 2003 have been fully considered but they are not persuasive.

11. With regard to applicant's argument that "the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art," it should be noted that this statement is not supported by either 35 U.S.C section 103 or MPEP section 2141. While applicant quotes sections from both 35 U.S.C section 103 and MPEP section 2141, neither include matter which corresponds to this statement. Therefore, applicant's argument is not persuasive, and the rejections are proper.

12. With regard to applicants ascertation "the Examiner has not met the requirements... in her consideration of the references," [emphasis added]. More careful consideration of the choice of words used by the applicant is respectfully requested.

13. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392,

170 USPQ 209 (CCPA 1971). Thus, the arguments are not persuasive and the rejections are proper.

14. With regard to applicant's argument that "Taking the idea of axial bond placement from Kohno would inevitably lead to the space inefficient 'outward' lead configuration," it should be noted that the orientation of the bond pads of the semiconductor chip of Kohno is used in the combination of Eide. There is no suggestion in the rejection that the outward lead configuration of Kohno be used in Eide. It is not clear why using the bond pad orientation of Kohno in Eide would "inevitably lead to" the outward bond teaching of Kohno. This aspect of Kohno is not relied upon in the combination of references. Therefore, the applicant's arguments are not persuasive and the rejection is proper.

15. With regard to applicant's "second" argument, it should be noted that Lin, not Kohno or Eide, teach the desirability and thus the obviousness of the combination of the rejection in above paragraph 7. Therefore, applicant's arguments are not persuasive, and the rejection is proper.

16. In response to applicant's "third" argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392,

170 USPQ 209 (CCPA 1971). Thus, the arguments are not persuasive and the rejections are proper.

17. With regard to the applicant's "fourth" argument, it should be noted that the applicant should cite specific portions of the rejection with which to disagree. While the applicant states "there is no suggestion or motivation...," proper motivation has been included for all combinations. For example in paragraph 7, both motivations of "in order to simplify a layout of bond pads" and "in order to provide external electrical connections to the device as stated by Lin in column 2, lines 44 – 50" have been provided. It is not clear why the applicant believes any of the suggestions or motivations fail. Therefore, the arguments are not persuasive and the rejections are proper.

18. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the suggestion to combine each of the references can be found in the rejection of the respective claims, above, and in previous office actions. Any allegation stating that there is no motivation to combine, without actually citing the motivation and why it fails, will not further

the prosecution of this application. Therefore, the arguments are not persuasive and the rejections are proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703) 308-6236. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
December 4, 2003